REMARKS

The Examiner objected to the drawings under 37 CFR 1.183(a). The Examiner stated "The limitation in claim 1, step (d) referring to 'removing a portion of said polysilicon line and a corresponding portion of said insulating sidewall layer in a contact region of said polysilicon line' (similar limitation in claim 12 step (d)) must be shown or the feature(s) canceled from the claim(s)."

In response, Applicants maintain these features are shown in Applicants drawings. Applicants respectfully point out that in Applicants Fig. 8 (see also paragraph 41), a trim mask island 230A cuts a gate stack 175 into gate segments 120 (see FIG. 9A and paragraphs 43 and 44) and that openings 235 in trim mask island 230A form contacts X2 and X3 (the semicircular notches of FIG. 9A) in gate segments 120 by removing portions of the polysilicon line (gate conductor 150, which is a layer within gate stack 175 and is polysilicon in one example, see 5B and paragraph 35) and insulating sidewall layer (spacers 180, which are silicon-nitride in one example, see FIG. 5B and paragraph 35). Contacts X1 and X5 of FIG. 9A are also formed by the same way, except edges 240 of the trim mask island 230A define the regions to of polysilicon line and spacers to be removed.

The Examiner objected to claims 12-18 because of the following informalities in claim 12 step (e) and claim 17 line: "In claim 12, step (e), ' a first PFET, a second PFET, a first NFET, second' should be 'said first PFET, said second PFET, said first NFET, said second' and in claim 17, line 1. '12' should be '14' because the 'capping layer' appears in claim 14."

In response, Applicants have amended claims 12 and 17 as the Examiner has suggested.

The Examiner rejected claims 1-8, 10 under 35 U.S.C. §102(b) as being unpatentable over Ohno (US 5,621,232).

The Examiner rejected claims 9 and 11 under 35 U.S.C. 103(a) as being unpatentable over Ohno in view of Jung (US 6,335,279).

Applicants respectfully traverse the §102(b) and §103(a) rejections with the following arguments.

35 USC § 102

As to claim 1, the Examiner states that "Ohno (Figs. 3-7 and text in col. 9, line 21 to col. 10, line 3) discloses the claimed invention by forming a polysilicon line 4b with sidewalls, gate dielectric 3b, insulating sidewalls 6, and silicide layer 7b on the sidewall of the polysilicon line in the doped silicon contact region 5b. FIG. 6 clearly shows that a portion of the polysilicon line and a corresponding portion of the insulating sidewall layer in a contact region of the polysilicon line have been removed."

Applicants contend that claim 1, as amended, is not anticipated by Ohno because Ohno does not teach each and every feature of claim 1. For example Ohno does not teach "removing a portion of said polysilicon line and a corresponding portion of said insulating sidewall layer to form a notch in said polysilicon line in a contact region of said polysilicon line; and after step (d), forming a silicide layer on said sidewall of said polysilicon line in said contact region."

Applicants respectfully point out that in Ohno FIG. 4, sidewall insulating film 6 is not removed, leaving gate electrode 4B intact. Next, in Ohno FIG 5 a titanium layer 9 is formed over the intact gate electrode 4B. Next, in Ohno FIG. 6 silicide layer 7B is formed. Formation of silicide layer 7B consumes some of the gate electrode 4B. Thus, thinning of the gate electrode is simultaneous with the formation of the silicide layer and the silicide layer is not formed "after removing a portion of said polysilicon line" as Applicants claim 1 requires.

Based on the preceding arguments, Applicants respectfully maintain that claim 1 is not unpatentable over Ohno and is in condition for allowance. Since claims 2-11 depend from claim 1, Applicants respectfully maintain that claims 2-11 are likewise in condition for allowance.

Relative to claim 2, Applicants maintain that there is no teaching in Ohno of "simultaneously removing additional sections of said polysilicon line and corresponding sections of said insulating sidewall layer to sever said polysilicon line into gate segments" as Applicants claim 2 requires.

Relative to claim 3, Applicants maintain that there is no teaching in Ohno of "wherein said polysilicon line is in the shape of a closed loop" as Applicants claim 4 requires.

Relative to claim 7, Applicants maintain that there is no teaching in Ohno of "between steps (a) and (b), forming another silicide layer on said top surface of said polysilicon layer" Ohno forms forming a single silicide layer on the etched polysilicon layer and does not also form another silicide layer on the polysilicon layer before it is etched into polysilicon lines.

35 USC § 103 Rejections

As to claim 9, Applicants have argued *supra* in response to the Examiners § 102(b) rejection of claim 1 that claim 1 is allowable, since claim 9 depends from claim 1, Applicants respectfully maintain that claim 9 is not unpatentable over Ohno over Jung and is in condition for allowance.

As to claim 11, the Examiner states that "Ohno is applied as above and does not disclose the polysilicon doped N-type or P-type nor an insulating capping layer over the top surface of the polysilicon. Jung (Figs. 3C-3F and text in col. 6, line 15 to col. 7, line 12) teaches that polysilicon 108 is doped, and capping layer 112, which has been simultaneously removed with the polysilicon. It would have been obvious to one of ordinary skill in the art at the time the invention was made to dope the polysilicon as taught by Jung in Ohno's process to form a conductive layer of the proper resistivity, and a capping layer to protect the lower layers and prevent current leakage."

Applicants contend that claim 11, as it depends from amended claim 1, is not obvious in view of Ohno over Jung because Ohno over Jung does not teach or suggest every feature of claim 11. For example, Ohno over Jung does not teach or suggest "step (d) including simultaneously removing corresponding sections of said insulating capping layer in said contact region of said polysilicon line." Applicants respectfully point out that Jung removes the capping layer simultaneously with removal of the polysilicon during formation of the polysilicon lines not after formation of the polysilicon line

Based on the preceding arguments, Applicants respectfully maintain that claim 11 is not unpatentable over Ohno over Jung and is in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR: Furukawa et al.

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